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Transmitted herewith for filing is the patent application (including Specification, Claims, Sequence Listing (if applicable) and Abstract, **17 pages**) of:

Inventor(s): **Jeffrey Zarnowski, Matthew Pace, Thomas Vogelsong, and Michael Joyner**

For : **A VIDEO BUS FOR HIGH SPEED MULTI-RESOLUTION IMAGERS**

***If a CONTINUING APPLICATION, please mark where appropriate and supply the requisite information below and in a preliminary amendment:*

[ ] *continuation* [ ] *divisional* **[X]** *Continuation-In-Part (CIP) of prior application Serial No.:* ***09/039,835***

*Prior application information:* *Examiner :*
*Art Unit :*

Enclosed are:

**[X]** **10 sheets** of informal drawings.

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## EXPRESS MAIL CERTIFICATE

DOCKET NO. : **201951/140**

APPLICANT(S) : **Jeffrey Zarnowski, Matthew Pace, Thomas Vogelsong, and Michael Joyner**

TITLE : **A VIDEO BUS FOR HIGH SPEED MULTI-RESOLUTION IMAGERS**

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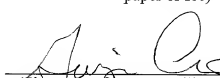

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**TITLE:** **A VIDEO BUS FOR HIGH SPEED MULTI-RESOLUTION IMAGERS**

**INVENTORS:** **JEFFREY ZARNOWSKI, MATTHEW PACE, THOMAS VOGELSONG, AND MICHAEL JOYNER**

**DOCKET NO.:** **201951/140**

# A VIDEO BUS FOR HIGH SPEED MULTI-RESOLUTION IMAGERS

This application is a continuation-in-part application of Application Serial No. 09/039,835 filed on March 16, 1998.

Field of the Invention:

This invention relates generally to busses and, more particularly, to a video bus for high speed multi-resolution imagers.

Background of the Invention:

An active pixel is a semiconductor device capable of converting an optical image into an electronic signal. Active pixels can be arranged in a matrix and utilized to generate video signals for video cameras, still photography, or anywhere incident radiation needs to be quantified. When incident radiation interacts with a photosite, charge carriers are liberated and can be collected for sensing. The number of carriers collected in a photosite represents the amount of incident light impinging on the site in a given time-period.

There are two basic devices with many variants, employed to collect and sense, charge carriers in a photosite. The two basic devices are photodiodes and photogates. Variants of photodiodes include, but are not limited to: Pinned, P-I-N, Metal-Semiconductor, Heterojunction, and Avalanche. Photogate structures include: Charge Couple Devices (CCD), Charge Injection Devices (CID) and their variants that include virtual phase, buried channel and other variations that utilize selective dopants. The selective dopants are used to control charge collection and transfer underneath and between the photogate(s) and the sense node.

The solid state imagers heretofore used have been dominated by CCD's because of their low noise as compared to Photodiodes and CIDs. The low noise advantage of CCD imagers is the result of collecting the photon generated charge at the pixel site and then coupling or shifting the actual charge to an amplifier at the periphery of the array. This eliminates the need for the long polysilicon and metal busses that degrade the signal with their associated resistance and capacitance. However, the low noise of the CCD requires the imager to be read in

a fixed format and once the charge is read it is destroyed. The requirement of coupling the collected photon charge from the pixel to the periphery amplifier (a.k.a. CTE), requires proprietary processing steps not compatible with industry standards CMOS or BiCMOS processes.

Solid state imaging devices have developed in parallel with CMOS technology and as a result all imager manufacturers developed their own proprietary processes to maximize imager performance characteristics and wafer yield. Specialized silicon wafer processing kept imager prices relatively high. Linear active pixel sensors have been commercially produced since 1985. Beginning in the early 90's the move to transfer the proprietary processes to an industry standard CMOS processes was on. The advantages of using an industry standard process include: competitive wafer processing pricing, and the ability to provide on chip timing, control and processing electronics. By the end of the year 1992 a 512 x 512 CMOS compatible, CID imager with a preamplifier and CDS per column had been fabricated. The imager could either be operated as a random access 512 x 512 CID, or all the columns could be summed together and operated as a linear active pixel sensor.

Area arrays utilizing active pixel sensors in which a photodiode or photogate is coupled to an output source follower amplifier which in turn drives a Correlated Double Sampling (CDS) circuit, where the two outputs of the CDS cell then drives two more source followers circuits that in turn are fed into a differential amplifier are shown in Patent No. 5,471,515. This uses source follower circuits, that typically have gains less than unity that vary from one source follower to another. The source follower gain variation is due to variations of FET thresholds. The source follower gain variation results in a pixel to pixel gain mismatch. Also, the active pixel sensors suffer gain variations due to the CDS circuit per column, when the CDS employs a source follower pair to drive its output. The resulting CDS signal and its corresponding offset can have different gains that are not correctable by the differential amplifier. Also, the source follower configuration of active pixel doesn't allow for binning of pixels.

The voltage mode of operation of prior art does not allow for binning, which, is the summation to two or more pixel signals at once.

What is needed is an imager device which has the low noise level of a CCD, the random access, and binning of a CID, and uniform gain and response from all pixels.

**Conventional Approaches to Industrial/Scientific Cameras**

The CCD sensor and camera electronics technology has evolved over the last 30 years to meet most of these demands. However the resulting cameras require a state-of-the-art, large pixel, multi-port CCD chip plus several extra chips and usually several circuit boards filled with electronics to accomplish this. Thus, the cameras cannot physically fit in certain applications, the power consumed is significant, and last but not least, the resulting cameras are far too expensive for many applications. The necessary recombination of the video data from several ports, further increases the video processing complexity and ultimately drives-up the cost and size of the video system.

Over the past several years, thanks to design rule shrinkage, image sensors using sub-micron CMOS process technology have become practical. By using CMOS technology for the sensor array itself, the problem of integrating extra circuitry on chip becomes straightforward. Elements such as A/D converters, timing generators, control circuitry and interface circuitry can easily be added. In addition, the operation of CMOS imagers is simplified by the elimination of the need for precise timing and level control of multiple clock required to drive the large capacitance transfer gates inherent in CCD's. Even with all of these factors, including the exceptional speed and pico-second gate delays of sub-micron processes, the analog video bandwidth per port hasn't changed much over the past 20 years.

Active pixel sensors (APS) have been proposed as the means to achieve the flexible benefits of CMOS cameras on a chip. Unfortunately, there are performance issues with the fundamental APS approach that limit its performance and functionality. While these limitations may be acceptable for consumer imaging applications, the demands of scientific and industrial applications have, up until now, been largely unmet by CMOS image sensors.

Brief Description of the Drawings:

Figure 1 is a prior art double polysilicon active pixel sensor;

Figure 2 is an active column sensor in accordance with this invention;

Figure 3 is an implementation of a pixel in accordance with the invention;

Figure 4 is a schematic illustration of a matrix of pixels connected to incorporate a full operational amplifier per pixel forming an Active Column Sensor;

Figure 5 is a view of a traditional CCD and CMOS sensor method of increasing video bandwidth with multiple ports;

Figure 6 is a view of a conventional method of driving a common video buss on an imager;

Figure 7 is a view of a high speed low noise video bus;

Figure 8 is a view of a bus for pixel reordering with a video processing block and a bus demultiplexor;

Figure 9 is a view of a bus for pixel interpolation for increased resolution; and

Figure 10 is a photograph of the invention.

Detailed Description of the Invention:

Before discussing the Active Column Sensor (ACS) circuit of Figure 2 of the present invention and described in conjunction with a discussion of ACS below, it will be useful to discuss the structure of a typical double-polysilicon active pixel sensor of prior art as shown in Figure 1.

In Figure 1 each pixel 50 has a photosite 60 that has an output FET 53 configured as a source follower. The source follower 53 is used to drive a subsequent signal conditioning circuitry, such as a Correlated Double Sampled Circuit (CDS) 55. The gain through a source follower 53 is less than unity. If the source follower located at the pixel site 50 has a given gain other pixels and their respective source followers in the same column may or may not have the same gain. The technique relies on wafer processing for all FETs in the array to have the same threshold. It isn't uncommon for FET thresholds, during operation, to vary by 100mV for a linear active pixel array.

The active pixel 50 of the prior art includes a photogate 60 and a transfer gate 62 that are used to couple photo generated charge onto the floating diffusion node 52 which is connected to the gate 56 of source follower 53. The drain of the output FET 53 is connected directly to a power supply rail VDD. The source follower output FET is in turn connected to the source 56 of row access FET 58. When the row access FET 58 is selected for reading, the FET 58 is turned on, allowing output FET 53 to be connected to a load 18 and drive the CDS circuitry 55 directly.

Figure 2 is a schematic diagram of a pixel 12 in accordance with the present invention in which the threshold variations from pixel to pixel of the prior art are eliminated. All pixels 12 in a row or column are in parallel and for simplicity only one is shown. Pixel 12 which can consist of any photosensitive device 10 is coupled to an FET 15 to isolate the pixel from the readout circuitry. The FET 15 is one FET of a differential input pair of an operational amplifier 30 that includes FET 24. For simplicity, in Figure 2 the amplifier circuit 30 is configured as a positive feedback unity gain amplifier. A feedback path 32 connects the output of amplifier 30 to input 17 which in this case is the gate of FET 24. The amplifier 30 could be configured to have gain, a full differential input or any operational amplifier configuration as the application required. The fixed gain of amplifier 30 eliminates the gain variability of the prior art. The output of the unity gain amplifier is connected to a Correlated Double Sampler (CDS) which is utilized to eliminate any fixed pattern noise in the video.

A current source 20 comprising an FET 22 has its source connected to a power source VDD and its drain connected to the sources of differential input FETs 15 and 24.

The drains of input FETs 15 and 24 are connected to a current mirror formed from FETs 26 and 28. The gates of FETs 26 and 28 are connected together and to the source 18 of input FET 15. The sources of FETs 26 and 28 are connected to a negative power source, VCC.

The source 30 of FET 24 is the output of the differential pair and is connected to CDS 34.

The input FET 15 could be either a N channel or P channel FET as the application requires. The pixel 80 could be either a photogate or photodiode.

Figure 3 is a detailed schematic of pixel 12 of the active column sensor shown in Figure 2. In this implementation a photogate 76 is utilized. Selection and reset of a sense node 72 is controlled by an FET 76. This Active Column Sensor pixel eliminates the separate selection/access FET 58 of prior art. All biasing and controls signals are supplied from the periphery of the pixel array.

The pixel can be operated in the following manner. An N type substrate is used and the substrate is biased the most positive potential, e.g. 5.0 volts. The photogate 70 preferably a layer of polysilicon is biased to an integrate level (e.g. 0.0 volts). The region 80 under the photogate 70 is depleted and as light strikes the immediate area, it will collect (integrate) photon generated carriers. Photogate 72 is been biased to the 5.0 volts and will not collect photon generated carriers during the integration because it is biased to the same potential as the substrate. Photogate 72 is biased by selecting control FET 76 with the reset/Select Control signal. In this configuration control FET 76 is a P channel FET that is selected by a negative signal relative to the substrate, for example 0.0 volts. During integration FET 76 is selected, the photogate is biased by the reset/select bias that preferably is at 5.0 volts. After a predetermined integration time period the pixel is read.

Reading the pixel is preferably accomplished in the following manner. The reset/select control is changed to 2.5 volts, causing the region beneath photogate 72 to be depleted, and the background level is read. Reset/select FET 76 is turned off by setting the reset/select control to 5.0 volts. Photogate 70 has its potential removed, and in this example 5.00 volts. Reading the signal will occur as the collected photon generated charge transfers from the region beneath photogate 70 to the region beneath photogate 72. The transferred photon generated charge modulates the gate of input FET 15, according to the amount of collected.

Fixed Pattern Noise (FPN) can be eliminated from the video information by utilizing CDS circuit 34. The first sample applied to the CDS circuit is the background level. The signal information is then applied to the CDS. The difference of the two signals provides for a fixed pattern noise free signal.

Figure 4 is a schematic diagram of an array of pixels in accordance with this invention. A plurality of pixels 90a, 90b, 90c form a first column of the array,

and similar columns 92a-c and 94a-c complete the array. Within each column, the pixels are connected with their output FETs in parallel, the combination forming the first one of the differential input pair of operational amplifier 30. In all other respects, amplifiers 30a, 30b and 30c are identical to Figure 2. Each amplifier 30 is connected to a CDS 34a, 34b, and 34c respectively. The outputs of CDS 34a, b, c are connected through column select switches 96a, 96b, and 96c, the common terminals of which are connected to output buffer 98 which can be a source follower, or a more complex signal conditioner as required by the specific application.

Industrial and scientific imaging applications require much higher performance and functionality than that required for consumer imaging products. Typical applications of this class of cameras include machine vision for automated inspection. Many of the applications require high readout speeds for video rate or even faster imaging without sacrificing image quality. In addition to image quality, the applications have come to demand greater functionality in the camera. Features such as flexible shuttering and electronic zoom, random access and selectable region of interest for maximizing frame rates and minimizing data storage (especially useful in tracking applications). Lowering the cost of machine system development is the recent advancement of single chip CMOS cameras. Newly developed CMOS cameras have all the flexibility previously listed; however, the analog video bandwidth per port hasn't changed from the traditional CCD, CID or Photodiode technologies. This invention relates to high speed video bus requirements in general and more specifically to solid state imagers.

The following section describes one embodiment of an on-board, high-speed bus that allows pixel rates exceeding those of single port CCD or APS devices in accordance with the present invention. This bus in combination with the highly parallel nature of amplifier per column techniques of CMOS sensors that provides both the functionality and high speed performance required for scientific and industrial applications. Experimental results of one embodiment of the present invention are also presented.

**1. Conventional Video Bus issues**

Most mega-pixel image sensors, including both CCD imagers and APS imagers, have a maximum pixel rate inadequate to meet the frame rate needs of industrial and scientific imaging. CCD devices are limited by both clocking rates and the speeds of the Correlated Double Sampled (CDS) circuitry. In addition the higher amplifier bandwidth required for higher pixel rates increases noise levels. With the column parallel nature of CMOS imagers, the amplifier and CDS can be run at the line rate rather than the pixel rate. The video bandwidth constraints come in terms of the multiplexing speed. CMOS imagers typically multiplex their signals onto a common analog video bus. The more signals that are multiplexed or switched onto the bus, the greater the capacitive load of that bus. Therefore, as more signals are connected to the bus, the bandwidth of the bus is reduced. Alternatively, greater power is needed to charge and discharge the bus with its associated capacitance to maintain bandwidth. In order to overcome the constraints, designers of CCD's and APS sensors have resorted to dividing up the imager into halves, quarters, or smaller groupings of sub-imagers, jammed together. The signal from each of these sub-imagers is brought out to its own port, as shown in Figure 5. Circuit 2 of Figure 5 is a video port that is replicated four times in this example. This approach has been used to provide high frame rate devices, or even to meet standard frame rates with large mega-pixel imagers. This adds system size, complexity, power and cost to handle the multiple analog amplifier chains. In addition, it is an extremely challenging task to balance the amplifier chains completely over all possible pixel rates and temperatures. This issue has become even more of a problem in recent years as imagers have grown larger, now up to full wafer size. The process variations across an array can lead to further balance problems, and even variations in noise characteristics, due to process variations across a wafer.

Often CMOS imagers have column parallel amplifiers that drive a common video bus. The common video bus is seen mostly as a capacitive load to each individual column amplifier as shown in Figure 6, circuit 14. In order for each amplifier to truly represent the pixel value onto the common video bus, the amplifier must charge or discharge the bus with in one pixel time constant. It must be stable long enough for a sample and hold circuit (or similar) to accurately

present the resultant signal to an A to D converter. A conservative engineer will want at least 5τ (tau or time constants) to accurately allow the video bus to settle the video value presented by each individual column amplifier. At higher video bus speeds the individual column amplifier, Figure 6, circuit 10, is unable to properly charge or discharge the video bus and results in a loss of contrast ratio. At higher pixel element rates where the contrast ratio is compromised, the individual column amplifier characteristic and the video switch characteristics begin to affect the resultant video. The individual column amplifiers will have slightly different offsets, Figure 6, circuit 10, with slightly different drive capabilities and each video switch, Figure 6, circuit 12, will have slightly different resistances and slightly different thresholds. This combination of column amplifier and video switch characteristics results in each column amplifier having different time constants relative to charging and discharging the video bus. The column amplifier and video switch are common to every pixel in that column. Thus, variations in the video switch characteristics result in what appears to be column based Fixed Pattern Noise (FPN). As more columns are added, each video switch adds more associated capacitance, Figure 6, circuit 14, due to the source and drain junctions of MOSFET or Bipolar transistors. The more columns added to the bus, the higher the total capacitance. Having identified the source of column based FPN and knowing that the pixel element rates cannot exceed the ability of the weakest column amplifier on the video bus a solution should be identifiable, without requiring high power amplifiers per column.

**2. High Speed PVS Bus**

A preferred approach over the segmented four port imager of Figure 5, would be to read out the imager four times faster on a single port. The ACS series of imagers incorporates a novel method of increasing the read rate of analog buses called the PVS bus. This speed increase has been achieved without increasing power consumption, and full video bandwidth is maintained even at the higher speeds. Common mode noise pickup is eliminated through the use of fully differential processing.

The high speed, low noise, low power analog PVS bus for imagers as shown in Figure 7 utilizes either standard sequential or random access decoders for selection of a particular column. In addition to selecting that column, it has the added preselection circuitry to pre-select the next three columns in the read sequence in parallel. The number of columns pre-selected can be scaled to meet the application requirements; four buses are used in Figure 7 for illustration purposes only. Preselection, circuitry 20 of Figure 7 is effectively a four input "or" Boolean logic function. Now instead of having separate quadrants of pixels as in Fig 5, there is only now only one. Preselection circuitry works in conjunction with parallel multiplexors, where the four columns are selected in parallel and are multiplexed to a separate differential video bus, Figure 7, circuit 26, for each column selected. Parallel multiplexors, Circuit 22, Figure 7. as shown in Figure 7, circuit 26 utilizes differential video per column and has two video buses for each column address. Therefore the total number of video buses is eight for Figure 7.

The purpose of selecting the current column and pre-selecting the next three columns is to allow the video bus to charge up to the proper value and settle prior to being demultplexed by as shown in Figure 7 circuit 24. By pre-selecting the three columns (or pixel time constants) ahead of time, the column video processing circuitry only has to drive the video bus at one quarter the actual pixel read rate (one-fourth the bandwidth) and therefore can be made smaller and lower power than they would otherwise have to be. Also, since each column is connected to only one out of every four columns the video bus has only one-fourth of the capacitance, because there are only one fourth of the transmission gates (or switches) to drive. As a result, each column selected also pre-selects the next three columns in sequence. The column selection sequence remains conventional, with out the need for post processing reconstruction of the original image required of multi-port imagers. The analog pre-charging is done at a one-fourth the bandwidth in Figure 7 than the prior art conventional single ended video bus and only the demultiplexing is done at the normal bandwidth.

The demultiplexor of Figure 7, 24 is a fully differential video bus designed to match the fully differential multiplexor of FIGURE7, circuit 26. Parallel multiplexors isolate all the different video buses. The timing for the demultiplexor circuit is generated via external control, an on chip counter, a small

shift register, or a controller. The demultiplexor timing control logic which in the implementation shown, is a counter with count decode logic. The video processing block that takes the differential video, provides gain, offset, filtering, or any video processing function. The demultiplexor timing control logic may decode the video bus circuit in any sequence that the application requires.

By utilizing the highly parallel nature of CMOS imagers and more specifically the fully differential video provided by the Active Column Sensor(ACS patent approved) technology, the PVS Bus is able to maintain near ideal MTF with high video bandwidths. The parallel nature of the PVS Bus also allows pixel reordering as shown in Figure 8, circuit 30. Pixel reordering can be column and/or row based. An example of row and column based reordering is the Bayer (or other) color filter. Figure 8 illustrates how the PVS Bus demultiplexor can go to another demultiplexor to reorder pixels as columns are read. The manner that the pixels are reordered can be row dependent, as is the case for color filters.

### 3. Combining Columns

Another useful approach to the column parallel nature of CMOS imagers is the ability to select multiple columns at once to average the video signal. This is possible because the column amplifiers of Figure 6, circuit 10 are identical in every detail and when more than one is selected at once the outputs from each amplifier try to drive each other and the result is that the two or more signals are averaged. This allows for higher speed of operation and it also gives a new method of binning or interpolating pixels. Binning is a term used to combine two or more pixel signals together. The higher speed of operation is due to two or more amplifiers driving the same video bus and as a result there is up to two times (or more) the ability to drive the same amount of capacitance. The binning is a result of combining two or more signals at the same time on the same video bus. The net result of combining multiple signals(a.k.a. averaging) onto the same bus is to effectively a multi-resolution imager.

This multi-resolution ability of the video bus can be used to effectively increase the resolution, through interpolation, not just decrease the resolution through binning. The increase of resolution is through the use of selectively

binning adjacent signals in between reading individual signals. In this manner, the time sequence would be for a conventional column orientated CMOS video bus, as in Figure 6, would be select column 1 and read the signal. Next in sequence leave column 1 selected and also select column 2. Read the combined (binned or averaged) signal and deselect column 1 and now only read column 2 signal. In this manner for every two adjacent signals read, a third interpolated signal can be read effectively increasing the resolution through interpolation. This allows a typical imager with 640 columns to have the effective resolution of 1279 pixels through interpolation.

**4. Row Binning**

The ACS series of imagers has been developed specifically for scientific and industrial applications and utilizes a bus in accordance with the present invention. The design incorporates the Active Column Sensor design approach that uses a unity gain amplifier per column with a selectable input transistor at every pixel along that column. An ACS technology imager will uniquely allow binning or interpolation along the row in a similar manner as the columns were just described above. The ability to bin (or average) is described in the ACS imager patent. Interpolation that the ACS technology uniquely allows, would utilize the just described method in the previous paragraph for the first row of video. The ACS imager would then select two adjacent rows of video (rows 1 and 2) and the above interpolation would be repeated and followed again by only selecting row 2 and rereading only row 2. In this manner a typical imager with 480 rows, can have an interpolated resolution of 959 rows.

What has just been described in the previous two paragraphs can be done at a much higher rate with the bus in accordance with the present invention described herein. Utilizing the PVS Bus where the current pixel being read and the next three(or more) pixels are pre-selected and pre-charging the remaining video buses in parallel, the column(pixel) averaging is done by the demultiplexor. Where the demultiplexor of Figure 7, circuit 24, is used to select adjacent pixels at the same time. Figure 9 illustrates in circuit 52 how simple the added circuitry can be to allow column to column interpolation.

While the invention has been described in connection with a presently preferred embodiment thereof, many modifications and changes may be apparent to those skilled in the art without departing from the true spirit and scope of the invention, which is intended to be defined solely by the appended claims.

CLAIMS

What is claimed is:

1. An multiplexed analog bus with a plurality of signal busses in parallel, wherein signals are selected onto the signal busses prior to being demultiplexed.

2. The bus as set forth in claim 1 wherein the selected signals are allowed to pre-charge each bus prior to reading.

3. The bus as set forth in claim 1 wherein the signals are selected in parallel along the column to pre-charge the busses prior to being demultiplexed.

4. The bus as set forth in claim 1 wherein the bus has the signals either demultiplexed on a substrate or externally.

5. The bus as set forth in claim 1 wherein the busses are multiplexed and demultiplexed in random or sequential order.

6. The bus as set forth in claim 1 wherein the busses are selected at once.

7. An imager comprising a differential video bus.

8. The imager as set forth in claim 7 wherein a differential video contains a desired signal on one node and a common mode noise on both.

9. The imager as set forth in claim 8 wherein the differential video contains different video signals on both nodes and common mode noise on both nodes.

10. An imager comprising analog processing to subtract the common mode noise.

11. An imager as set forth in claim 10 wherein analog bus can either be differential or single ended.

12. A video bus with multiple signals selected at once in parallel.

13. The bus as set forth in claim 12 wherein the video bus has multiple signals selected in sequence or in random.

14. A column to column interpolation by selecting two or more columns on the same video bus.

15. The column to column interpolation as set forth in claim 14, wherein the interpolation is performed by reading two or more signals separately and combined using the same video signals.

16. A column to column interpolation by selecting two or more analog busses for demultiplexing at the same time.

17. The column to column interpolation as set forth in claim 16 wherein multiple signal busses are demultiplexed onto the same node.

18. The column to column interpolation as set forth in claim 16 wherein the demultiplexion is in sequence or random

19. A row to row interpolation by selecting two or more rows simultaneously to be combined along the column.

20. The row to row interpolation as set forth in claim 19 wherein the row to row interpolation for active column sensors is accomplished by selecting two or more rows simultaneously and having their currents combined along the column.

21. The row to row interpolation as set forth in claim 19 wherein multiple row selection are in sequence or in random.

22. An interpolation along both the rows and columns at the same time by selecting two adjacent rows and two adjacent columns.

23. The row to row interpolation as set forth in claim 22 wherein two or more row and column selections are in sequence or random.

24. A column to column binning by selecting two or more analog busses for demultiplexing at the same time.

25. The column to column binning as set forth in claim 24 wherein multiple signals busses are demultiplexed onto the same node.

26. The column to column binning as set forth in claim 24 wherein multiple signal busses are demultiplexed in sequence or random

27. A row to row binning by selecting two or more rows simultaneously to be combined along the column.

28. The row to row binning as set forth in claim 27 wherein the row to row binning for active column sensors is accomplished by selecting two or more rows simultaneously and having their currents combined along the column.

29. The row to row binning as set forth in claim 27 wherein multiple row selection are in sequence or in random.

30. A binning along both the rows and columns at the same time by selecting two adjacent rows and two adjacent columns.

31. The binning as set forth in claim 30 wherein two or more row and column selections are in sequence or random.

## ABSTRACT

An analog video bus architecture that utilizes the column parallel nature of CMOS imagers and more specifically Active Column Sensors, that eliminates the need for multi-port imagers, by increasing the useable bandwidth of single port imagers. An adaptation of this invention allows for either binning or interpolation of pixel information for increased or decreased resolution along the columns and more specifically for ACS imagers binning or interpolation along the rows. In this bus, the single video bus is replaced by multiple video buses and instead of selecting only one column for reading multiple columns are also pre-selected in-order to pre-charge the video bus. The video buses are then de-multiplexed back on to one port at the desired element rate. This architecture utilizes the column oriented video bus of CMOS imagers. It divides the large video bus capacitance by the number of video buses used. In addition, it allows multiple pixel time constants to precharge the video bus. The best commercially available imager designs now claim 40 MHz per analog port and suffer from reduced signal to noise ratios. To overcome this fundamental bandwidth limitation, imager designs in the past have had to increase the number of video ports per imager to achieve high frame rates. Multiple ports per imager breaks the focal plane into segments that are typically reassembled via post processing in a host computer. The other problem with multiple ports is each segment of the imager will have its own offsets and resultant Fixed Pattern Noise (FPN). PVS-Bus™ eliminates the objectionable segmentation and simplifies high-speed system design. Also, by utilizing the column parallel nature of CMOS video buses a method and improved method of using the PVS-Bus of binning and interpolation is described which results in increased frame rate, and for decreased or increased resolution.

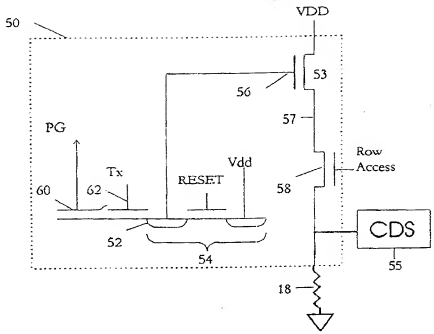



Figure 1
Prior Art

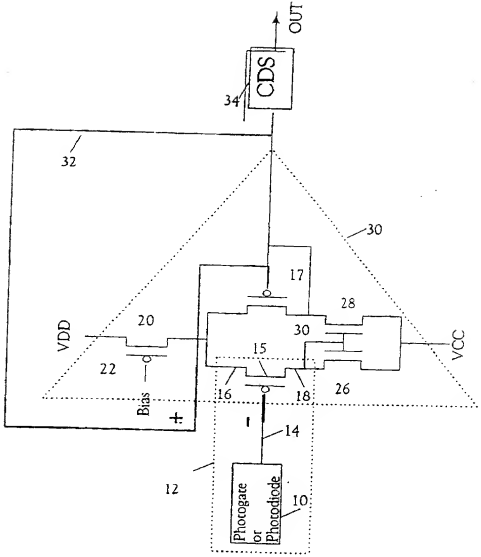

OUT
CDS
34
32
30
17
28
VDD
20
30
VCC
15
22
Bias
16
18
26
+
-
14
12
Photogate
or
Photodiode
10

Figure 2

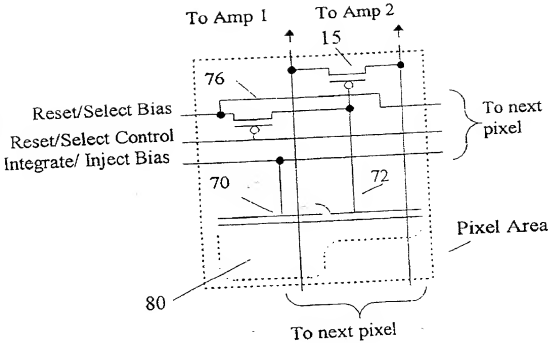

To Amp 1
To Amp 2
15
76
Reset/Select Bias
Reset/Select Control
Integrate/ Inject Bias
To next pixel
70
72
Pixel Area
80
To next pixel

Figure 3

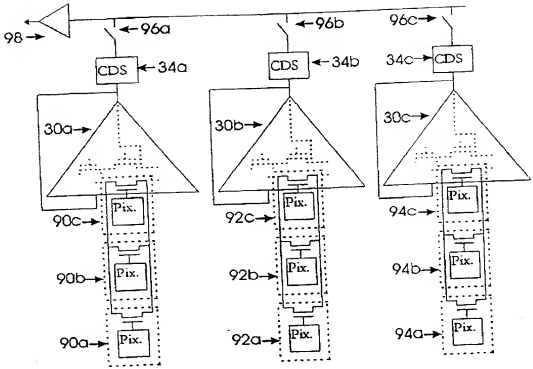

98
96a
96b
96c
CDS
34a
CDS
34b
34c
CDS
30a
30b
30c
Pix.
90c
92c
94c
90b
92b
94b
90a
92a
94a

Figure 4

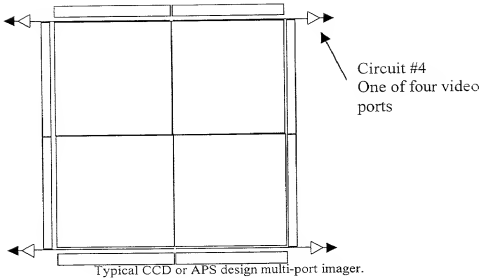

Circuit #4
One of four video
ports
Typical CCD or APS design multi-port imager.

FIGURE 5

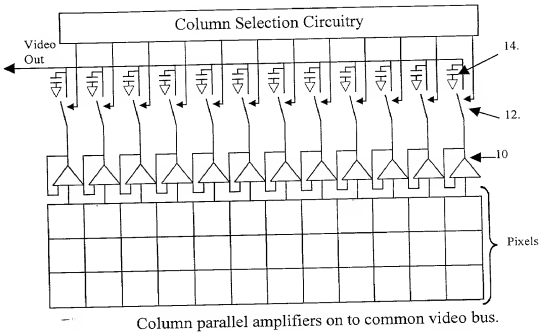
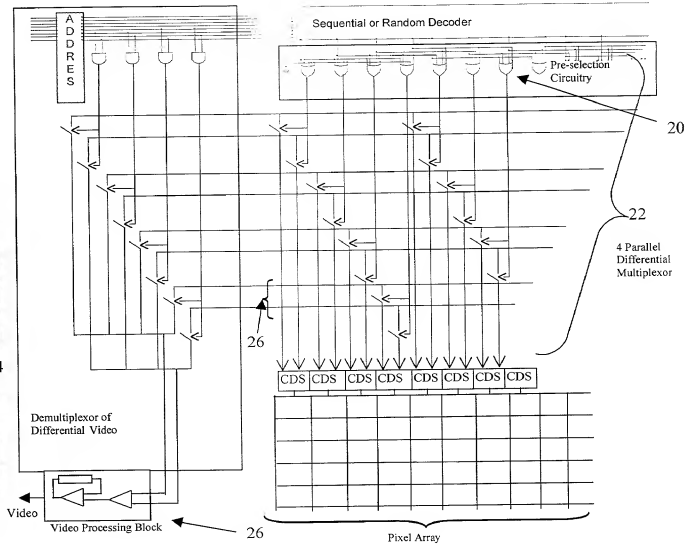

Column Selection Circuitry
Video Out
14.
12.
10
Pixels
Column parallel amplifiers on to common video bus.

FIGURE 6




PVS Bus that eliminates multi-ports for high speed black and white

FIGURE 7

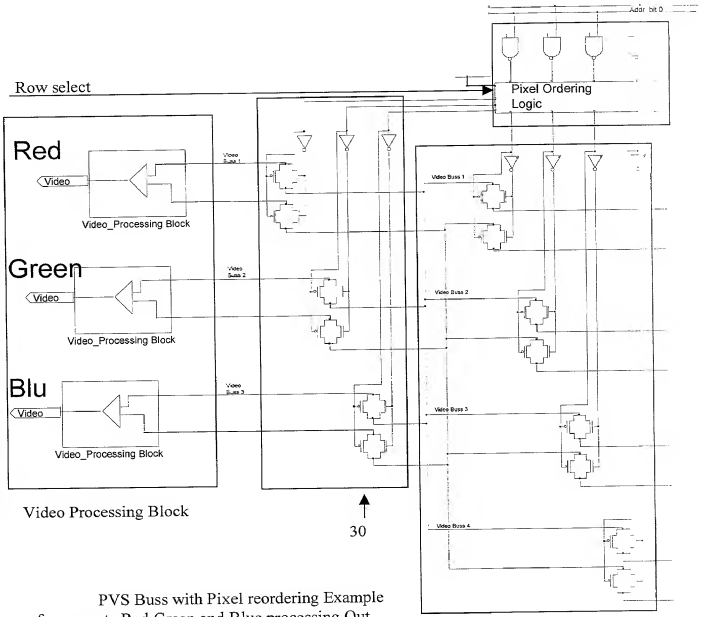
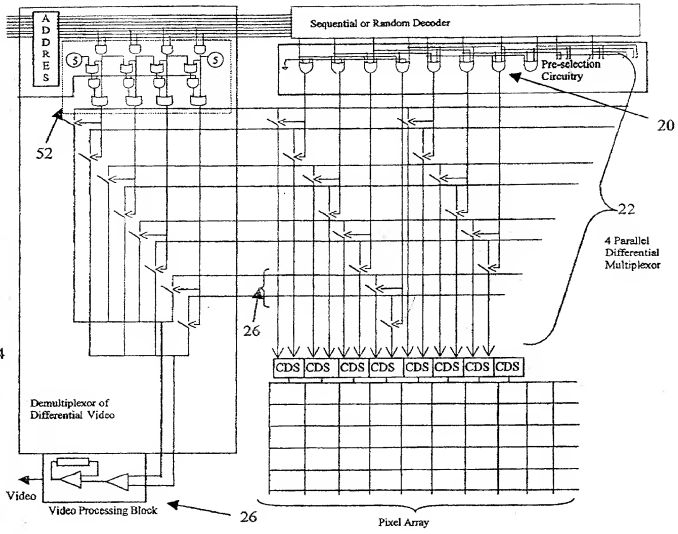

Addr bit 0
Row select
Pixel Ordering Logic
Red
Video
Video_Processing Block
Green
Video
Video_Processing Block
Blu
Video
Video_Processing Block
Video Buss 1
Video Buss 2
Video Buss 3
Video Buss 4
Video Processing Block
30
PVS Buss with Pixel reordering Example for separate Red Green and Blue processing Out
PVS Bus Demultiplexor

FIGURE 8




PVS Bus that eliminates multi-ports for high speed black and white

FIGURE 9

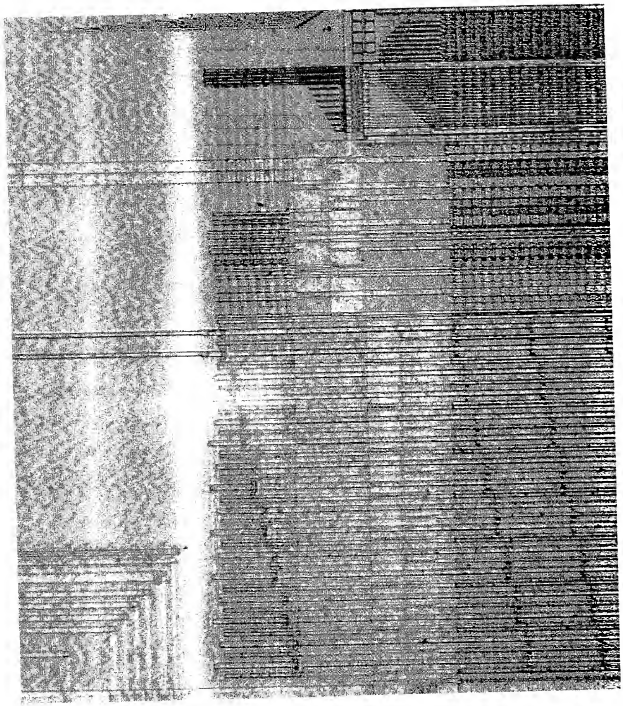


FIGURE 10

| COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY (Includes Reference to PCT International Applications) | ATTORNEY'S DOCKET NUMBER 201951/140 |
|---|---|

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

**A VIDEO BUS FOR HIGH SPEED MULTI-RESOLUTION IMAGERS**

the specification of which (check only one item below):

[X] is attached hereto.

[ ] was filed as U.S. Patent Application Serial No. _____ on _____ and was amended on _____ (if applicable).

[ ] was filed as PCT International Application No. _____ on _____ and was amended under PCT Article 19 on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specifications, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations. § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. 119:

| COUNTRY (IF PCT, indicate "PCT") | APPLICATION NUMBER | DATE OF FILING (day, month, year) | PRIORITY CLAIMED UNDER 35 USC 119 |
|---|---|---|---|
| | | | [ ] YES [ ] NO |
| | | | [ ] YES [ ] NO |
| | | | [ ] YES [ ] NO |

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application(s) and the national or PCT International filing date of this application:

PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATIONS DESIGNATING THE U.S. FOR BENEFIT UNDER 35 U.S.C. 120:

| U.S. APPLICATIONS | | STATUS (Check One) | | |
|---|---|---|---|---|
| U.S. APPLICATION NUMBER | U.S. FILING DATE | PATENTED | PENDING | ABANDONED |
| **09/039,835** | **March 16, 1998** | | **X** | |
| | | | | |

| PCT APPLICATIONS DESIGNATING THE U.S. | | | | | |
|---|---|---|---|---|---|
| PCT APPLICATION NO. | PCT FILING DATE | U.S. SERIAL NUMBERS ASSIGNED (if any) | | | |
| | | | | | |
| | | | | | |

| COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY (Continue) | ATTORNEY'S DOCKET NUMBER **201951/140** |
|---|---|

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. **Michael L. Goldman, Registration No. 30,727; Gunnar G. Leinberg, Registration No. 35,584; Dennis M. Connolly, Registration No. 40,964; Edwin V. Merkel, Registration No. 40,087; Georgia Caton, Registration No. 44,597; Grant E. Pollack, Registration No. 34,097**

| Send Correspondence to: | **Gunnar G. Leinberg, Esq.**<br>**NIXON PEABODY LLP**<br>**Clinton Square, P.O. Box 1051**<br>**Rochester, New York 14603** | Direct Telephone Calls to:<br>(name and telephone number)<br>**Gunnar G. Leinberg**<br>**(716) 263-1094** |
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| | RESIDENCE & CITIZENSHIP | CITY | STATE/FOREIGN COUNTRY | COUNTRY OF CITIZENSHIP |
| | POST OFFICE ADDRESS | P.O. ADDRESS | CITY | STATE & ZIP CODE/CTRY |

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statement may jeopardize the validity of the application or any patent issuing thereon.

| SIGNATURE OF INVENTOR 201 | SIGNATURE OF INVENTOR 202 | SIGNATURE OF INVENTOR 203 |
|---|---|---|
| **UNSIGNED** | **UNSIGNED** | **UNSIGNED** |
| DATE **1/24/2000** | DATE **1/24/2000** | DATE **1/24/2000** |
| SIGNATURE OF INVENTOR 204 | SIGNATURE OF INVENTOR 205 | SIGNATURE OF INVENTOR 206 |
| **UNSIGNED** | | |
| DATE **1/24/2000** | DATE | DATE |